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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ZHU, JOHN X	

ART UNIT	PAPER NUMBER
2858	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

TH

Office Action Summary	Application No.	Applicant(s)	
	10/756,749	TINNEMANS, PATRICIUS ALOYSIUS JACOBUS	
	Examiner	Art Unit	
	John Zhu	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-13,15 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-13,15 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Response to communications filed on 6/27/2007.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1,4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jagiella et al. (5,489,888) in view of Jostlein (5,315,259) and Blake et al. (5,444,597).

With respect to claims 1 and 6, Jagiella discloses a capacitive detection assembly comprising at least one electrode (Fig. 1, element 2), a cable having a first conductor (element 7) connected to the electrode at a first end, and connected to an AC source (element 100) at a second end, a second conductor (element 8), and a controller (element 6) for supplying a measuring signal to capacitively detecting an object.

Jagiella does not explicitly disclose the electrode being arranged adjacent the support structure to detect the object on the support structure, or a second AC source connected to second conductor wherein the controller controls the second AC to provide an AC voltage having a second amplitude and phase substantially equal to the AC voltage supplied by the first AC source, or in another embodiment, the second AC source controlled by the first AC voltage source such that the first AC source multiplies the second AC voltage by unity.

Blake discloses a method and apparatus for wafer detection using capacitive means wherein the electrode (Fig. 3, 22) is adjacent to the support structure (base 16) to detect the wafer 12. As both the references of Jagiella and Blake utilizes non-contact capacitive type detection system, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the support structure configuration as taught by Blake for the purpose of detecting a presence of a wafer on a wafer support (Claim 2).

Jostlein discloses that it is well known in the art of capacitive sensing to apply a second AC voltage to an outer conductor similar in magnitude and phase as a first AC voltage being supplied to an inner conductor (Column 3, lines 45-57). Although Jostlein does not explicitly disclose the second voltage source being controlled by the first source at first AC source multiplies the second AC voltage by unity, it would have been obvious to include a design to control the second voltage supplied via a first voltage supply for the purpose of simple design and cost effectiveness since only one source could be the used as an independent source while the other source (i.e. VCVS) depends on it.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the second AC voltage as taught by Jostlein for the purpose of eliminating the effect of stray capacitance on probe measurements (Column 3, lines 55-59).

With respect to claim 4, Jagiella further discloses the second conductor (8) partially enclosing the first conductor (7).

4. Claims 10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jagiella in view of Jostlein, Blake and Saeki et al. (5,557,215).

With respect to claims 10 and 17, Jagiella discloses providing/controlling a first AC voltage (element 100) to the electrode 3 via first conductor 7 for capacitively detecting the object.

Jagiella does not disclose detecting an object on a support structure, applying a DC source to provide a clamping force, or providing a second AC voltage to a second conductor having an amplitude and phase substantially the same as the first AC voltage.

Blake discloses a method and apparatus for wafer detection using capacitive means wherein the electrode (Fig. 3, 22) is adjacent to the support structure (base 16) to detect the wafer 12. As both the references of Jagiella and Blake utilizes non-contact capacitive type detection system, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the support structure configuration as taught by Blake for the purpose of detecting a presence of a wafer on a wafer support (Claim 2).

Jostlein discloses applying a second AC voltage to an outer conductor similar in magnitude and phase as a first AC voltage being supplied to an inner conductor (Column 3, lines 45-57).

Saeki discloses a DC source (element 46) applying a DC voltage to clamp a semiconductor wafer to a support (Column 7, lines 13-17).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the second AC source and voltage as taught by Jostlein for the purpose of eliminating the effect of stray capacitance on probe measurements

(Column 3, lines 55-59) and further obvious to modify Jagiella to include the DC source on the wafer as taught by Saeki for the purpose of securing a wafer on a platform.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jagiella et al. (5,489,888) in view of Jostlein (5,315,259) and Saeki et al. (5,557,215).

With respect to claim 15, Jagiella discloses providing/controlling a first AC voltage (element 100) to the electrode 3 via first conductor 7 for capacitively detecting the object.

Jagiella does not disclose applying a DC source to provide a clamping force, or providing a second AC voltage to a second conductor having an amplitude and phase substantially the same as the first AC voltage.

Jostlein discloses applying a second AC voltage to an outer conductor similar in magnitude and phase as a first AC voltage being supplied to an inner conductor (Column 3, lines 45-57).

Saeki discloses a DC source (element 46) applying a DC voltage to clamp a semiconductor wafer to a support (Column 7, lines 13-17).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the second AC source and voltage as taught by Jostlein for the purpose of eliminating the effect of stray capacitance on probe measurements (Column 3, lines 55-59), and further obvious to modify Jagiella to include the DC source on the wafer as taught by Saeki for the purpose of securing a wafer on a platform.

6. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jagiella, Jostlein and Blake as applied to claim 1 above, and further in view of Saeki et al. (5,557,215).

With respect to claims 2 and 3, Jagiella as modified discloses all aspects of the claim except a first conductor is connected to a DC source that is in series with the first AC source to provide a clamping force via DC voltage to an object which is a wafer.

Saeki discloses a DC source (element 46) applying a DC voltage to clamp a semiconductor wafer to a support (Column 7, lines 13-17).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the DC source on the wafer as taught by Saeki for the purpose of securing a wafer on a platform for self-bias voltage measurements.

7. Claim 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Jagiella in view of Jostlein, Blake and Neukermans et al. (4,654,581).

With respect to claim 7, Jagiella discloses a capacitive detection assembly comprising at least one electrode (Fig. 1, element 2), a cable having a first conductor (element 7) connected to the electrode at a first end and an AC source (element 100) connected at the second end, a second conductor (element 8), and a controller (element 6) for supplying a measuring signal to capacitively detecting an object.

Jagiella does not explicitly disclose the electrode being arranged adjacent the support structure to detect the object on the support structure, a second AC source connected to second conductor wherein the controller controls the second AC to provide an AC voltage having a

second amplitude and phase substantially equal to the AC voltage supplied by the first AC source, or an illumination system constructed to provide a beam of radiation.

Blake discloses a method and apparatus for wafer detection using capacitive means wherein the electrode (Fig. 3, 22) is adjacent to the support structure (base 16) to detect the wafer 12. As both the references of Jagiella and Blake utilizes non-contact capacitive type detection system, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the support structure configuration as taught by Blake for the purpose of detecting a presence of a wafer on a wafer support (Claim 2).

Jostlein discloses that it is well known in the art of capacitive sensing to apply a second AC voltage to an outer conductor similar in magnitude and phase as a first AC voltage being supplied to an inner conductor (Column 3, lines 45-57). Although Jostlein does not explicitly disclose the second voltage being from a separate source or the same source, it would have been obvious to include either design system for the purpose of reduced costs or simpler design as they both produce the same result of providing a second AC voltage equal in magnitude and phase.

Neukermans discloses a capacitive sensing system for a lithographic apparatus comprising an illumination device 7 providing a beam of radiation and ridge/fingers (Fig. 9) to provide alignment.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the second AC voltage as taught by Jostlein for the purpose of eliminating the effect of stray capacitance on probe measurements (Column 3, lines 55-59), and further modify Jagiella to include the illumination system of Neukermans for

the purpose of properly detecting and aligning a mask and a wafer during photolithography (Abstract, lines 1-4).

8. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jagiella, Jostlein, Blake and Neukermans as applied to claim 7 above, and further in view of Leeser (US PG Pub no. 2002/0008954 A1) and Tanimoto et al. (4,870,452).

With respect to claims 8 and 9, Jagiella as modified does not disclose controlling actuators to move when clamping force is above a predetermined value, and determining a clamping force to provide a max value for acceleration.

Leeser discloses using a capacitance value determined by the electrodes (Fig. 1, 112,114) with the wafer on the surface and without the wafer on the surface to derive an optimal voltage that maintain an optimal chucking force upon the wafer (paragraph 0013). Since a chucking force is directly related to the capacitance value measured, it is obvious to not induce the wafer to sufficient stressing (whether due to acceleration, gravity, etc.) to cause the force exerted on it to be greater than the predetermined chucking force.

Tanimoto discloses controlling actuators (Fig. 1, element 42) to move the support structure with the wafer.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the determination of chucking force based on capacitance/chucking force relationship as taught by Leeser for the purpose of finding the limits of stress parameters which could cause harmful effects to the wafer and to control actuators as taught by Tanimoto for the purpose aligning wafers within the limits of those stress parameters.

9. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jagiella, Jostlein, Blake and Saeki as applied to claim 10 above, and further in view of Barnes et al. (5,670,066).

With respect to claim 11, Jagiella as modified discloses all aspects of the claim except determining a first capacitance with the object present and a second capacitance without the object present and storing at least one capacitance in memory.

Barnes discloses a workpiece positioning system comprising measuring a first and second capacitance before and after an object is placed on the chunk (Claim 2) and storing the measured capacitance in a memory in the controller (Column 5, lines 5-6).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the first and second capacitance and storing as taught by Barnes for the purpose of determining the presence of a workpiece prior to an electrostatic force being applied.

10. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jagiella, Jostlein, Blake and Saeki as applied to claim 10 above, and further in view Leeser (US PG Pub no. 2002/0008954 A1) and Ishida (US PG Pub no. 2003/0072122 A1).

With respect to claim 13, Jagiella as modified discloses all aspects of the claims except for determining a clamping force of the support structure based on the difference in capacitance between the support structure with and without an object present, deriving a maximum acceleration allowed, and moving the structure when an acceleration is less than the max acceleration allowed.

Leeser discloses measuring a capacitance without a wafer present and a capacitance value when a wafer is on the chuck (paragraph 0013), and monitors the capacitance value to derive an optimal chucking voltage that maintains an optimal chucking force upon the wafer (paragraph 0013/paragraph 0027, 'capacitance can also be used to estimate this net force'). Since a chucking force is directly related to the capacitance value measured, it is obvious to not induce the wafer to sufficient stressing (whether due to acceleration, gravity, etc.) to cause the force exerted on it to be greater than the predetermined chucking force.

Ishida discloses the relationship between chucking force and maximum acceleration (paragraph 0055).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include the determination of clamping force via capacitance measurement as taught by Leeser for the purpose of derive an optimal chucking voltage that maintains a optimal force on the wafer and further obvious to modify Jagiella and Leeser to include the relationship between chucking force and maximum acceleration for the purpose of setting the limits of stress the wafer can endure before the chucking force breaks down.

With respect to claim 12, Jagiella as modified does not disclose moving the structure after comparing the clamping force to predetermined minimum clamping force. As the chucking force necessary to hold the wafer in place is already determined, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jagiella to include comparing the force to a predetermined minimum clamping force to hold the structure in place

while moving for the purpose of finding the limits of stress parameters which could cause harmful effects to the wafer.

Response to Arguments

11. Applicant's arguments with respect to all claims have been considered but are moot in view of the new ground(s) of rejection.

With respect to the arguments concerning claim 1 and 10, the reference of Blake has been added to show capacitively detecting a wafer on a support structure.

With respect to the argument that Jagiella does not inherently teach providing a DC voltage to provide a clamping force on an object (page 10, paragraph 1, lines 4-6), Saeki has been added to show a DC voltage used to provide a clamping force.

With respect to the arguments concerning claim 7, the difference between claim 7 and claim 1 is that claim 7 includes an illumination system constructed to provide a beam of radiation, Neukermans disclose a capacitive detection system in a photolithography system and contains a illumination system constructed to provide a beam of radiation.

With respect to the arguments concerning claim 8 and 9, the reference of Tanimoto is used to teach actuators in a lithography system.

In response to the argument concerning claim 11 that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the

knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, as all the references combined deal with capacitively detecting a wafer, there exist motivation to combine references to improve the detection system by detecting and aligning.

With respect to the argument concerning claims 12 and 13 that the references do not disclose, teach or suggest moving the support structure, Ishida and Leeser are added to show that the structure holding the object is positioned to move within limits of the maximum chucking force.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Zhu whose telephone number is (571) 272-5920. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Hirshfeld can be reached on (571) 272-2168. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JZ

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